**CHAPTER 3**

**CADENCE design tools**

**3.1 Introduction**

The intentions for this manual is to serve as an introduction to the Cadence de-sign environment and describe the methodology used when designing integrated circuits. The department is not giving courses in Cadence but in integrated circuit design so only the minimum knowledge needed to run the libraries of Cadence can be gained from this manual. Also this manual describes the environment currently at the department which is Cadence version 4.45 in conjunction witch a Design Kit from AMS (Austria Mikro Systeme International AG) which contains a set of rules and designs for a 0.35 g m CMOS process.

For a more thorough understanding of Cadence the extensive on line manual set is recommended. These are accessed from any of the tools by pressing the help button. More information about the topics in the first two chapters can be found in the manuals Design Framework II Help and Cadence Application Infrastructure User Guide.

The Cadence tool kit consists of several programs for different applications such as schematic drawing, layout, verification, and simulation. These applications can be used on various computer platforms. The open architecture also allows for integration of tools from other vendors or of own design. The integration of all this tools is done by a program called Design Framework 11 (DFW).

**3.2 Cadence User Interface**

In Cadence the user interface is graphic and based on windows, forms, and menus. The main windows of DFW are:

Command Interpreter Window (CIW) is controlling the environment. Other tools can be started from here and it also serves a log window for many applications.

Library Manager gives a view of the design libraries and the different constructions that exists therein.

Design Window (DW) shows the current design. It is possible to have several DW opened at the same time with different, or the same, tools.

Text Window (TV) shows text. It can be a log or report that was asked for, or an editor.

The menus in Cadence are mostly pull-downs, i.e. the menu will appear when the title are clicked with the left button on the mouse. There are also pop-up menus that appear in the background of the design window on a middle button press. The forms are used for entering some specific information that is needed by the function called, the size of a transistor for instance.

**3.3 The Design Process**

The design tools have a common structure of the designs. It is hierarchical and consists of libraries, views, and instances.

**3.4 Libraries and Views**

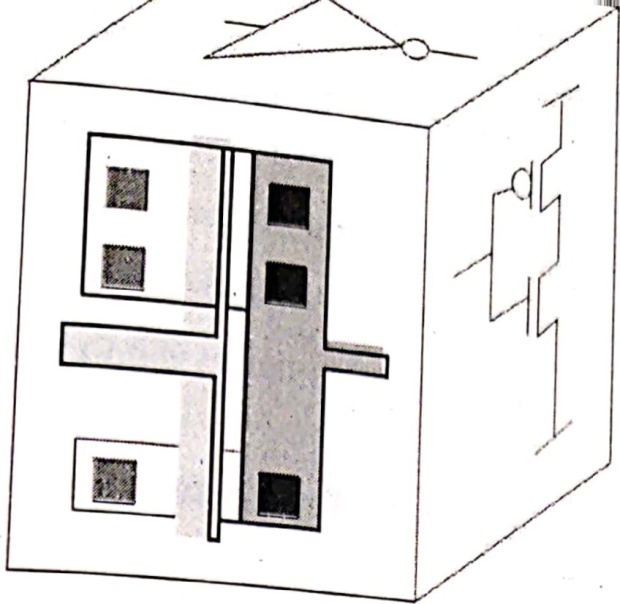
All design data in Cadence are organized in libraries. There are Reference Libraries which contains basic building blocks usable in the construction and Design Libraries which embodies the current design. Every library consists of cells and their different views, as in figure 1.1. A cell is a database object which forms a building block, an inverter for instance. A view represents some level of abstraction of the cell. It can be a schematic drawing, layout, or maybe some functional description.

Fig 3.l: An inverter cell with three views: layout, schematic, and symbol.

**3.5 Instances and Hierarchy**

The main reasons for using hierarchical designs are to save design time and minimize the size of the data base. Say that a design would need 500 gates of the same type. Then instead of building it 500 times, it is designed once and then used were it is needed. In this way one cell can be used (not copied) several times and each such use is called an instance of the cell. In order to be instantiated every cell needs a symbol view which acts as a handle to the cell it represents. Only the symbol is shown when a cell is instantiated.

Thus by creating more complex structures by instantiating simple instances a hierarchical design is formed. It is possible to move up and down and work on a selected level in the hierarchy. When a design is opened, the highest level is the default one.

**3.6 The Technology File**

Since there are different semiconductor processes (with different set of rules and properties), Cadence has to know the specifications for the one that is to be used. This information is stored in a set of files called Technology Files which exists on different locations on the system. When a library is created it is therefore connected to a specific technology.

The technology files contain information about:

* Layer definitions: Conductors, contacts, transistors
* Design rules: minimum size, distance to objects
* Display: Colours and patterns to use on the screen.
* Electrical properties: resistance, capacitance.

The technology files are usually supplied by the silicon vendor, which is to fabricate the design, along with some libraries of standard cells and 10 pads that can be used by the designer. Such a collection is called a Design Kit.

**3.7 The SKILL Programming Language**

When a command is performed, from a form or a menu, the system is executing functions written in the SKILL language. SKILL is developed by Cadence and is based on Lisp. The Cadence tools are using SKILL for internal communication and for the tool design communication.

SKILL is also accessible for the designers. Commands can be written in the CIW-window or placed in command files for execution. it can be used for simple tasks like executing a command or building more complex functions to perform various tasks. 

**3.8 The Design Flow **

The abbreviated flow shows some of the steps in designing integrated circuits in the Cadence environment.

Create the design

Analyze the design

Create layout

Verification

The step Create the Design consists of drawing schematic views of all cells and blocks. The schematic view contains transistor symbols, and maybe other component such as resistors and capacitances and wires connecting them. From the schematic view symbol view is created almost automaticaly so that the cell can be used on a higher level in hierarchy.

The step Analyse the design includes functional verification (simulation) of the design on a schematic level.

The third step, Create Layout, is done in a Layout Editor. Here the final semiconductor layers are represented by different colours. All the cells and blocks used have the size they will have on the final chip.

The last step is Verification of the design. The layout is examined for violations against the geometric or electrical rules, and to verify the function of the physical implementation.

**3.9 Schematic and Symbol tools**

To create the schematic the tool Virtuoso Schematic Composer is used. This editor is an interactive system for building schematics by instantiating some basic components (transistors, capacitances, etc.) and to connect them to each other. The values (properties) of the components can be edited to suit the specifications. Text and comments can also be included. The editor will also create symbols of the cells so that they can be used in other part of the construction.

**3.10 Simulation**

The simulation tool is started directly from the schematic editor and all the necessary net-lists describing the design will be created. A simulation is usually per-formed in a test bench, which is also a schematic, with the actual design included as an instance. The test bench also includes signal sources and power supply. By using parameters for the Properties of the components used it is possible to quickly analyse the design for a wide range of variables. The simulator is run from within Affirma Analog Circuit Design Environment which is a tool that, handles the interface between the user and the simulator.

The current version of Cadence used at the department (4.45) uses the Affirma spectre Circuit Simulator. The simulator offers a wide range of analyses (Dc, frequency sweep, transient, noise, etc.) and the results can be presented graphically and be saved.

**3.11 Layout Tool**

The Virtuoso Layout Editor is used for drawing the layout. A layout consists of geometrical figures in different colours. From the size and colour of these figures it is later possible to generate the final mask layers which are used in the fabrication of the design. It is possible to include other cells by instantiating their layout views.

To verify that the layout fulfils all electrical and geometric rules a Design Rule Check (DRC) program is used. This manual will describe Assura Diva verification which can be called upon directly from the layout editor. This tool will mark any error in the design and can also extract (i.e. convert to a net-lists) the layout so it can be simulated.

**3.12 Place and Route**

The final stage of the construction of a large design is called place and route. This is the process when all the different components of the chip is placed on its locations and connected to each other. Since a design can easily consist of thousands of connection points it would be tedious and time consuming to do the connections manually. The designer might also want to try various alternatives in placing the components, output buffers, memory structures, amplifiers, etc.

The place and route tool that will be described later in this manual is named Envisia Silicon Ensemble. It is a very potent program that that can place and route a very large design while respecting some design constraints (restrictions on delay and size) at the same time. 

Usually Silicon Ensemble is used for Standard Cell designs - this is when all the cells are of the same height so they can be placed in contact (abutted) with each other - but it can handle other structures.

**CHAPTER: 4**

**DRIVE CIRCUIT & SENSE AMPLIFIER**

**4.1 Drive circuit:**

The driver circuit is one of the basic components in the memory design circuit. The job of the driver is to bring the bit line and bit line bar to ground potential for the further this the bit line and bit line are being charged maximum supply voltage Vdd. With precharge circuit it was get charged and after that it gets discharged. It is also known driver. The driver gets enabled by the word enable which is in the connected in the part. It is two nmos transistors are being connected back to back with fascinated with also two inverters in the upper part. First of all, two logics are given to the two points of the junction of the nmos. i.e., 0 and 1. The bit line which is nearer to the logic 0 it gets discharged first after that its logic gets inverted. Like this way the bit line and bit line bar gets discharged to the ground. With this kind of operation the bit line and bit line bar gets discharged. Its main job is to provide low impedance path to the ground. So the voltage difference between bit line and ground, bit line bar and ground is zero. So another data can be easily retrieved by the memory cell when more no of data is to be accessed.

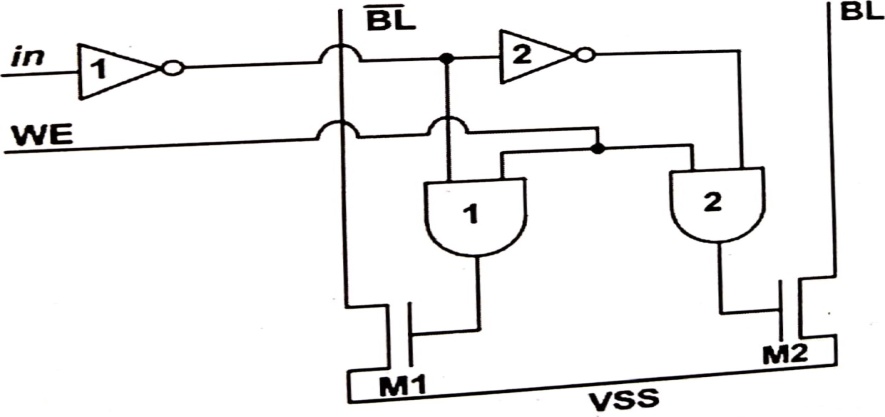


Fig.4.1 simple Write Driver using and gate

**Advantages:**

1. With the driven circuit we able to bring the bit line and bit line bar to the ground potential by adding a low voltage and a high voltage at two points of the cross coupled inverters
2. From this we can get initialisation conditions of the circuit.
3. Full modification is not needed by the designer
4. We can get full description of the circuit
5. Its description is easy

**Disadvantages:**

1. The FETs (Field Effect Transistor) are being used have much higher on resistances, which difficult to get and higher cost also.
2. Switching speed of this circuit is also less.
3. Implementation of the circuit is also little bit complicated

**4.2 Sense Amplifier circuit:**

Sense amplifiers are the vital component in the memory design. The job of sense amplifier is to sense the bit line and bit line bar for proper monitoring action. It improves the read and write speed of the memory cell. It's another job is to reduce the power needed for the operation. The sense amplifiers primary job is to amplification of the voltage difference is being produced on the bit line and bit line bar at the time of operation. As it has the important job in the memory so it has different circuits for the operation.

As we know that in SRAM operation we don't need refresh of the memory for the process, so the sense amplifiers non-destructive at the time of operation. As the column multiplexers are connected in the memory cell at that time multiplexer should choose one sense amplifier for the single input. We can get a proper use of the sense amplifier in the designing circuit. We have used the unsynchronised sense amplifier for simplicity. To be designed:

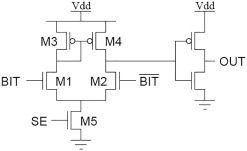


Fig.4.2 Sense Amplifier Used

**Advantages:**

1. Although it can feet in the column pitch, s there is no need of column selection device in the circuit. It reduces propagation delay.
2. There exists a virtual short circuit across the bit line and bit line bar by which it is independent of current distribution in the circuit.
3. The delay in the circuit does not get affected by the bit line and bit line bar capacitance.
4. The bit line current is gets discharged through this capacitance.

**Disadvantages:**

1. It has negligible signal swing.
2. Bit line voltages decreases cross talk in between bit line and ground potential.
3. Power dissipation is also more.

**CHAPTER: 5**

**Column I/O**

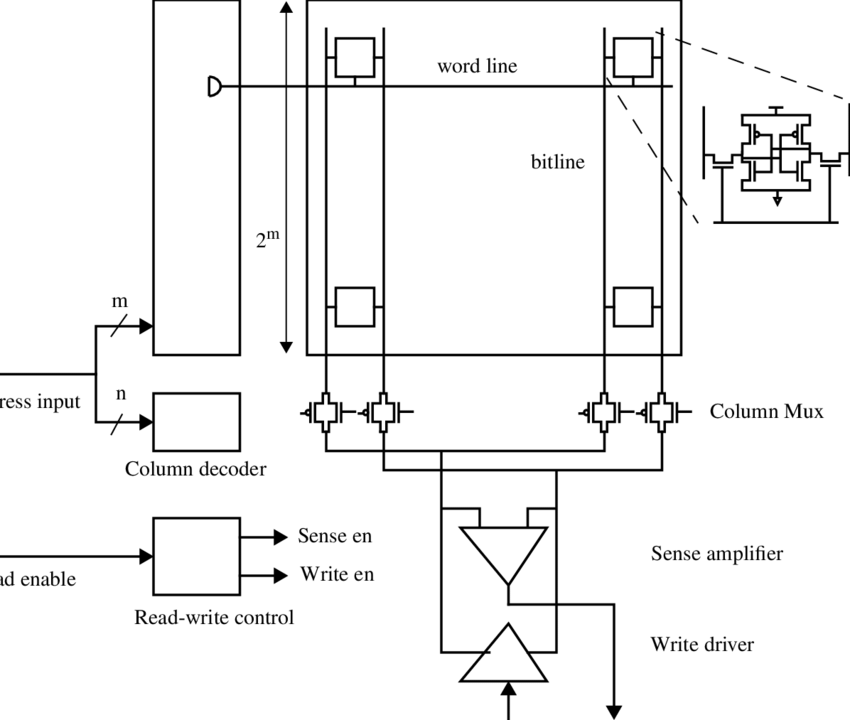


Fig.5.l column circuit

**I Column I/O:**

Circuits that perform read and write on the array are column I/O

* Bit line load

1. Can be static or precharged
2. Proper configuration depends on amplifier design

* For read

1. Bit lines must start at around Vdd
2. Swings should be small for fast operation
3. Involves MUX and sense amplifier design

* For write

1. Need to drive one of the bitlines to Gnd
2. MUX and write driver design
3. Often use different I/O lines for read and write

**II Column Ml-TX:**

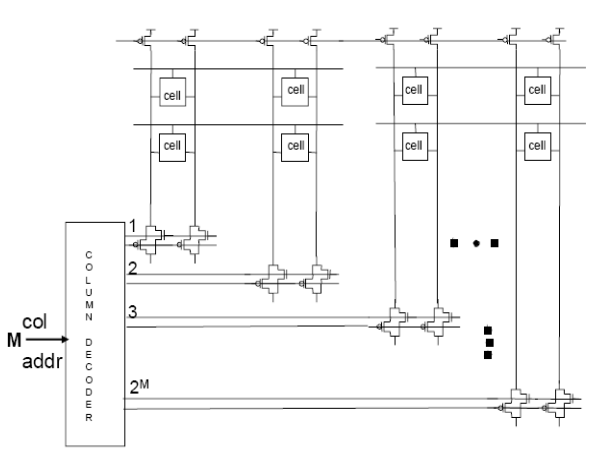
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Fig.5.2 Column Decoder with I/O 

Since the requirements for read and write are different can use separate read and Write 10 lines. Have PMOS access for the read 10 lines, since the read happens near Vdd. Have NMOS devices for the write 10 lines, since you need to drive bitlines to Gnd.

**CHAPTER 6**

**PLAN OF WORK**

As of now we have on working on the understanding the schematics of a basic 6T SRAM.

Now in the upcoming semester we are going to complete this project by June 2022.

The work to be carried out in the semester is as follows:

* We have implemented a single port SRAM, by implementing a dual port SRAM both read and write operations can be done simultaneously.
* The complete array which includes peripheral components such as memory bit cell, write driver circuit, pre-charge circuit, Sense amplifier are designed and integrated with the software.
* The proposed work operated with 0 to IV, Iv is the supply voltage and consumes 49.94 mw power. The power consumption mainly depends upon the number of transistors and the type of technology in use (in this case 45nm), the SRAM is designed and implemented in standard TSMC 45nm technology and Cadence virtuoso tool is used for schematic.

The final result of the project is:

* The present work analyses the power calculations and area analysis for different widths in different technologies.
* In the first instance 6T SRAM cell is designed to operate under normal conditions; further analysis is carried out for different ‘w’ values in order to understand the behaviour of SRAM cell.
* PVT analysis for the 6T cell is performed because this is the heart of whole design which helps in understanding the variations in power consumption of memory cell for variations in process, temperature and voltages.

**REFERENCE**

1. M. U. Khan, M. Zeeshan, U. Gulzar, M. Muneeb, Z. Abbasi and U. B. Abbasi, "Nanotechnology (45 nm) based Low power and High performance 4x4 Multiplier based on Six Transistors (6T) Full Adder & 2T XNOR Gate," 2021 International Conference on Computing, Electronic and Electrical Engineering (ICE Cube), 2021, pp. 1-6, doi: 10.1109/ICECube53880.2021.9628269.
2. Pratikshs Kulkarni, Punithra H M, Nalina H D, Preethana M, Kajal Kumari, 2020, Low Power 6T SRAM Design using 45nm Technology, INTERNATIONAL JOURNAL OF ENGINEERING RESEARCH & TECHNOLOGY (IJERT) NCCDS-2020 (Volume8-Issue 13).